Abstract

A low power and low cost RFID tag reader is designed and implemented. The reader is designed to work with ISO 11785 compliant RFID tags [1] and provides a reading range of 7 cm. In order to check the industrial compatibility, we have demonstrated the reader functionality on Low Frequency (LF) Half Duplex (HDX) TIRIS cards manufactured by Texas Instruments. An efficient hardware algorithm is proposed to smartly detect the presence of the RFID Tag. The proposed power saving architecture reduced the power consumption by nearly 30%. The RFID reader was successfully interfaced with the Vertex II Pro FPGA kit and the data from the RFID tag was stored in the FPGA memory to demonstrate the software interfacing. The low cost implementation of the RFID reader can be integrated on a chip and can be used in applications such as animal tracking, inventory management, library management, authorised access and many more.

1 System Architecture Overview

The system is based on a sequential function principle also called HDX (Half Duplex) separating the transponder powering (charge) and transponder data transmission (read) phase. Further details of the HDX protocol can be seen in TI RFID reference guide [2]. The typical data low bit frequency is 134.7 kHz; the typical data high bit frequency is 123.7 kHz as own in Figure 1. The low and high bits have different durations, because each bit takes 16 RF cycles of the corresponding frequency. The data stored in a tag typically consists of 128 bits. Different start/stop bytes and end bits are used, to allow secure distinction between Read Only and Read/Write Transponder. Data encoding is done in NRZ mode (Non Return Zero).

A reader for the above protocol should be able to first power up the tag and then be able to receive the transmitted signal from the charged tag. The reader must demodulate the incoming FSK modulated signal and extract the corresponding clock for sampling of bits.

Figure 1 shows the major building blocks of the designed reader. Square wave generator fed to the antenna coil resonates at 134.7 KHz charges the tag for 50ms and for next 20 ms the data is received from the tag. TXCT Generator provides the control for this half duplex communication. The received RF signal from the tag, after proper signal conditioning, is fed to filter banks and FSK detector for demodulation. The BIT SAMPLER derives the clock needed for sampling the output of FSK detector from the same RF signal. Power Saving Module reduces power consumption in the absence of tag. We detail each block in the following sections.

2 Design of Hardware Modules

2.1 Square Wave Generator

A 134.7 KHz square wave generator is used as the Radio Frequency source. NE555 is operated in bi-stable multivibrator mode of operation to produce a square wave of corresponding frequency. As the resonant frequency of designed coil is 134.7 KHz we can forego the need for a
sinusoidal source and use a square wave instead. This helps in decreasing design complexity as described in later sections. Since the output frequency is quite high 134.7 KHz, this can lead to significant glitches in power supply due to current peaks. Hence we used a hefty bypass capacitor ~1000uF near the 555 timer chip.

2.2 TXCT Generator

For implementing the Half Duplex Protocol (HDX) a control signal is used to decide when to radiate (energise tags in the vicinity) and when not to radiate (i.e. be in reading mode). This control signal is hereby referred as TXCT. In order to comply with standard adopted (ISO 11785) we need an at least 50 ms long charge phase and at least 20 ms long read phase. This TXCT has been implemented using a 555 timer in bi-stable multivibrator mode. TXCT is ANDed together with RF Source and fed to RFID reader coil. Had the RF source been sinusoidal, an analog multiplier would have been needed to modulate the radiation. The use of square wave as the RF source becomes advantageous as purpose of an analog multiplier is now served by an AND gate, further reducing the power consumption.

2.3 Reader Coil Design

A series resonant circuit was designed to function as the reader coil. Series resonant circuit was chosen as it provides maximum current and maximum coupling at resonance. The circuit is made resonant at the carrier frequency of 134.7 KHz. We used a rectangular multilayer loop as shown in Figure 3 to make the inductor coil.

2.4 FSK Demodulator and Detection

The RF_IN signal received from the antenna contains the FSK modulated data transmitted by the tag. In order to demodulate the FSK signal FSK demodulator and detector were designed using two high Q band pass filters followed by envelope detectors and comparator as shown in Figure 4. Altemately one may use PLL based FSK demodulator [3] but it increases the design complexity.
The two BPF designed were each centred at one of the two frequencies present in the FSK signal i.e. 123.7 KHz (bit ‘1’) and 134.7 KHz (bit ‘0’).

The Envelope detector design is very crucial to the correct detection of the incoming FSK modulated bit stream. We used a simple diode detector. The FSK rate of the signal is approximately 8 KHz. So the value of resistance and capacitor should be chosen so that the discharge time is sufficiently less than the bit interval i.e. around 125 ms. Also the discharging time should be large enough so that it maintains the envelope of the incoming signal. We chose the discharging time to be equal to approx 33ms. The two envelope amplitudes obtained from the two envelope detectors are fed to a comparator which is used for detecting the corresponding bit. The output of the comparator is the DATA_STREAM and Figure 6 shows the DATA_STREAM displayed on a digital oscilloscope.

2.5 Bit Sampler

As described in the protocol structure 16 RF cycles are used for the transmission of one bit. A suitable clock is needed to sample the value of the bit from the DATA_STREAM at appropriate instant. The function of the counter designed was to give a pulse after counting 13 RF cycles and remain high for next 2 RF cycles (counting 14 and 15). After this, the counter goes to 0 and the process continues. The counter output thus serves as the sampling clock of the DATA_STREAM. The design is shown in Figure 7 and corresponding snapshot from the digital oscilloscope is shown in Figure 8. Since the FSK demodulator output was prone to glitches during bit transitions, the BIT_SAMPLER was suitably designed to take this into account as its low to high transition was forced on the instants far from the bit transition instants i.e. when the corresponding bit’s certainty in the DATA_STREAM was assured.

The counter input RF_IN is active during both the charge phase of the tag and the read phase of the tag. Hence, it is necessary to disable the counter during the charge phase. This is done by setting TXCT to the enable of the counter.

3 Power Saving Scheme

As the system always tries to detect/read the RFID tag, there is unnecessary power wastage in the system when the tag is absent. It is not necessary to give continuous power to the all the constituent blocks of the reader such as the demodulator, RF generator etc when the tag is not present. Hence, in order to save power, we propose a novel algorithm and hardware to detect the presence of the RFID tag and subsequently give continuous supply to all the blocks of the circuit in the presence of the tag.
The proposed hardware is shown in Figure 9. It checks the presence of a RFID tag by periodically powering up the circuit. If tag is not found, the circuit continues to be in sleep mode. If tag is present, the power is given continuously until the tag leaves the RF field, whereupon the circuit goes back to the sleep mode. A 2 Hz clock with $T_{on} = 200\text{ms}$ and $T_{off} = 300\text{ms}$ is generated. Thus, the circuit is on for 40\% of the time and off for 60\% of the time when the tag is not present. However, duty cycle can be reduced upto 14\% ($50\text{ms}$ of charge phase and $20\text{ms}$ of read phase). This clock controls power supply of the reader when the tag is not present. The presence of a tag is known by the occurrence of BIT_SAMPLER. The BIT_SAMPLER is fed to a 4-bit counter. After a count of 8, a trigger for mono-shot is generated and the counting is disabled. The mono-shot output is fed to the input of a D-flip flop clocked by TXCT. The mono-shot output is kept high for 25ms to allow the high bit to be latched by TXCT. During the next read cycle, the counter is enabled again to detect the presence of the tag and correspondingly trigger the mono-shot output to go high. When the tag is removed, the counter does not trigger the mono-shot and the output remains low. Correspondingly, a low is latched by the D-flip flop, detecting the removal of tag. The output Q of the flip-flop controls the power supply of the reader, when the tag is present. To switch the power supply of the reader circuit, a standard BJT could not be used due to insufficient current capacity. The design thus employs the use of a power transistor 2N3055. To control the power supply of the reader blocks OR of output of flip-flop Q and the generated 2 Hz clock is used. This is fed to the base of the power transistor to switch the power supply of the reader blocks according to the changes in the control signals. The entire circuit is provided as the load at the emitter by connecting the power supply of the reader blocks to the emitter of the power transistor. With the proposed power saving module the power consumption of the system drops to half in sleep mode. Hence, with the specified frequency and duty cycle parameters we can save up to 30\% power.

4 Design of Software module

The hardware of circuit provides the bit stream inside the tag (DATA_STREAM) and the sampling clock for the data (BIT_SAMPLER).

A module is required which takes this bit sequence, retrieves the data present in the tag and uses it for further processing. We demonstrated one form of processing by validating data read for RFID tag against a database.
The Vertex II PRO XC2VP30 FPGA kit meets the necessary requirements to create the above mentioned interface. The signals DATA_STREAM, BIT_SAMPLER and TXCT are taken as input through the Expansion Header Pins. The signal TXCT is checked to detect whether the current cycle of the reader is charge cycle or read cycle. At the onset of every charge cycle, the retrieved data is set as null to prevent the data (if present) from the previous read cycle to be detected in current cycle. Further, the rest of the signals DATA_STREAM and BIT_SAMPLER are checked for valid input only during the read cycle. This prevents unscrupulous detection of data bits.

In the read cycle, the BIT_SAMPLER is used to sample the incoming data and store in a temporary register. On the retrieval of the entire 128 bit sequence, the retrieved data of the tag is verified against the data present in the ROM. If the data on tag matched the data stored in the ROM, a VALID signal is sent out of the FPGA pins showing that the tag has been successfully verified. Else, an INVALID signal is sent to the FPGA pin.

**Conclusion**

A robust, low cost and low power RFID reader is designed and implemented. A snapshot of prototype (without the FPGA kit) is given in Figure 10. The designed reader when tested with commercially available ISO 11785 compliant RFID tags from Texas Instruments a reading range of upto 7 cm was achieved. The whole design was implemented with a total cost of less than 10$. Commercially available readers are available in the range of 100-200$. The power consumption by the reader with no tag present was approximately 650 mW, saving upto 30% of the power.

**References**

[1] RFID Handbook Fundamentals and Applications in Contactless Smart Cards and Identification, Klaus Finkenzeller